

FIG. 1A

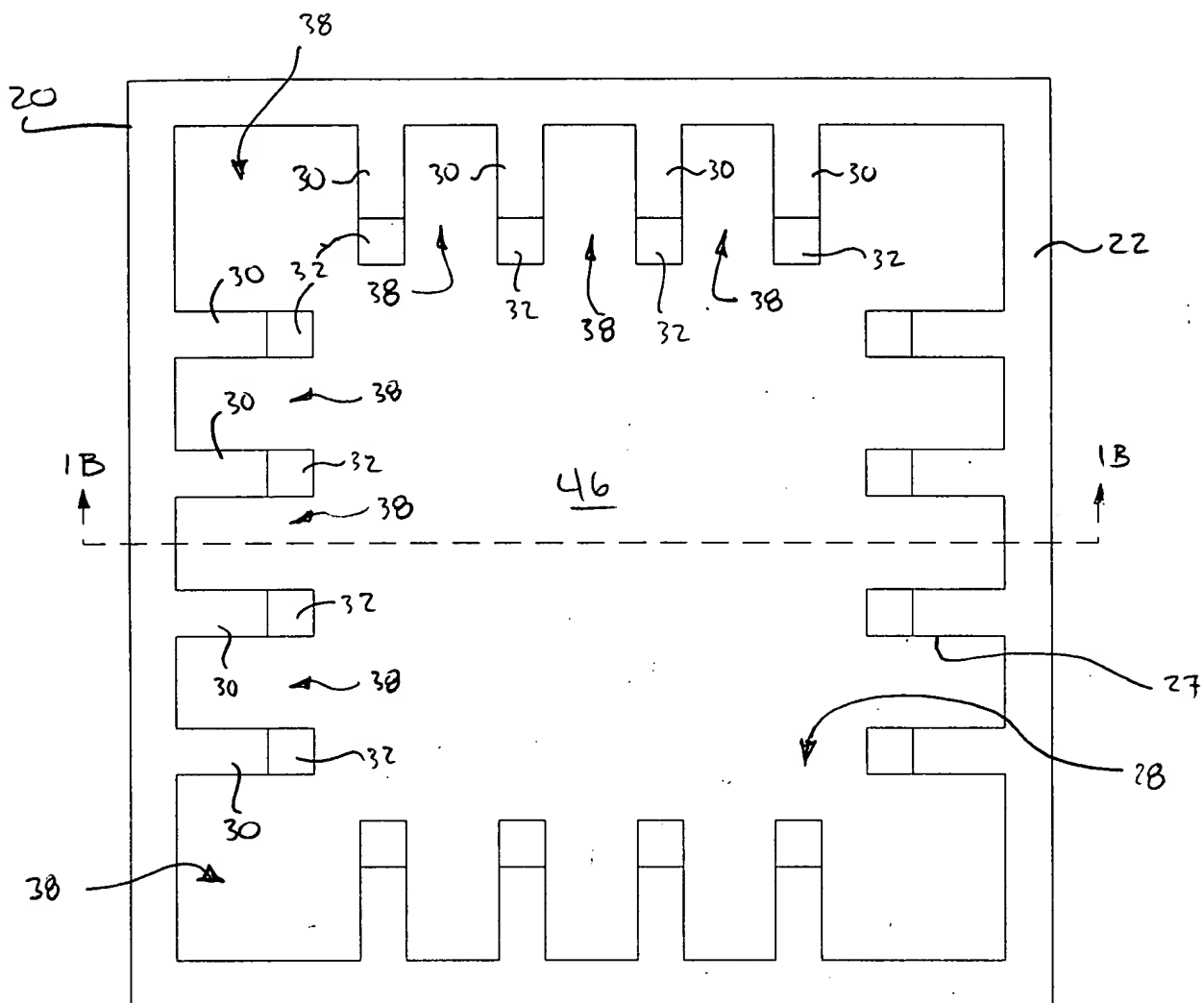


Fig. 1A

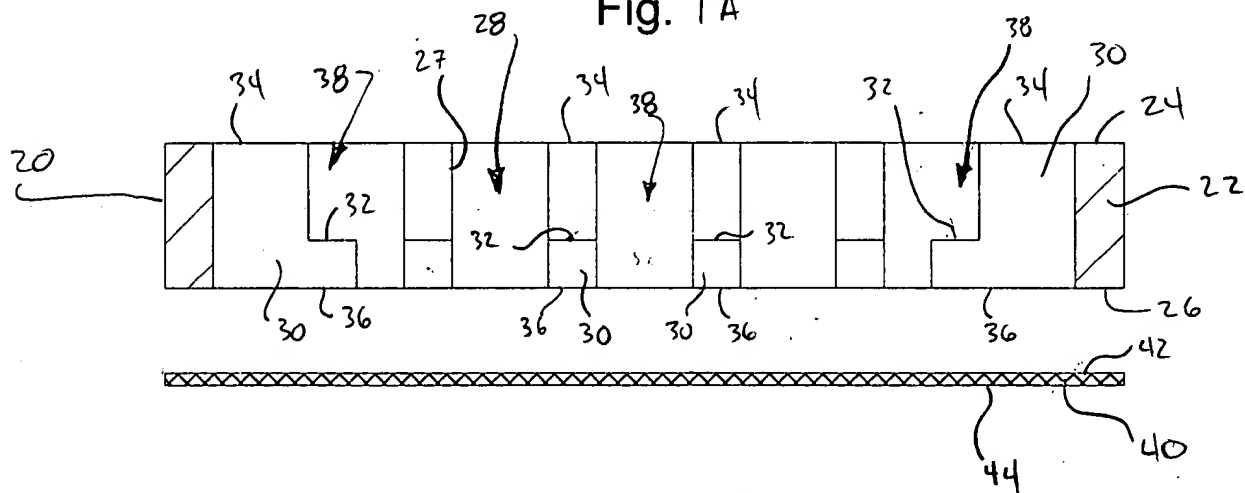


Fig. 1B

19FIG. 1A

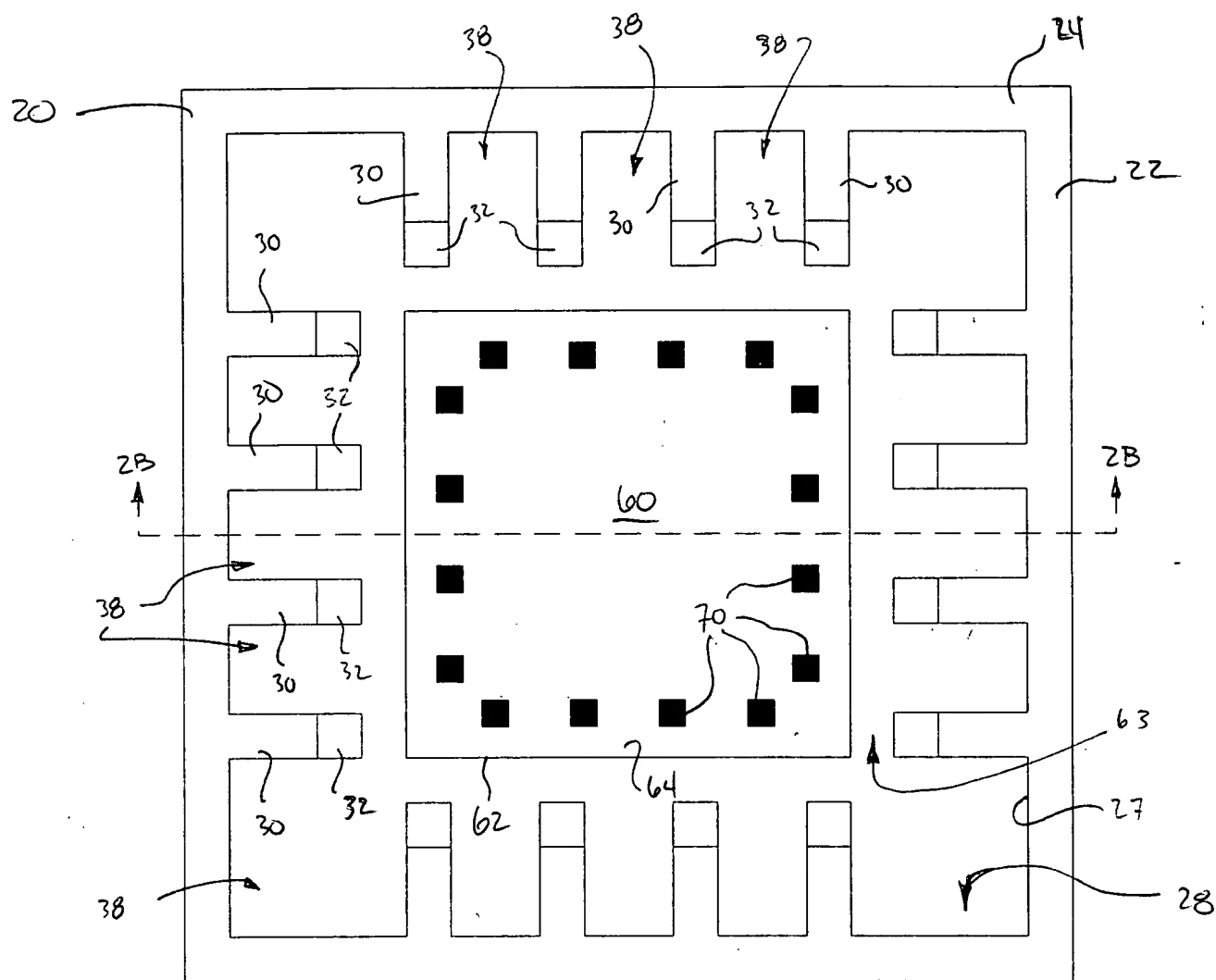


Fig. 2A

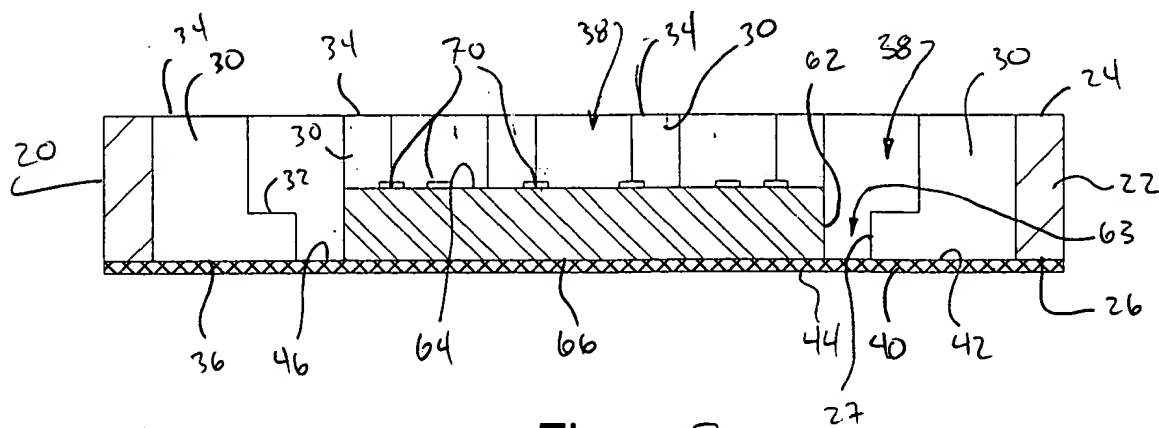


Fig. 2B

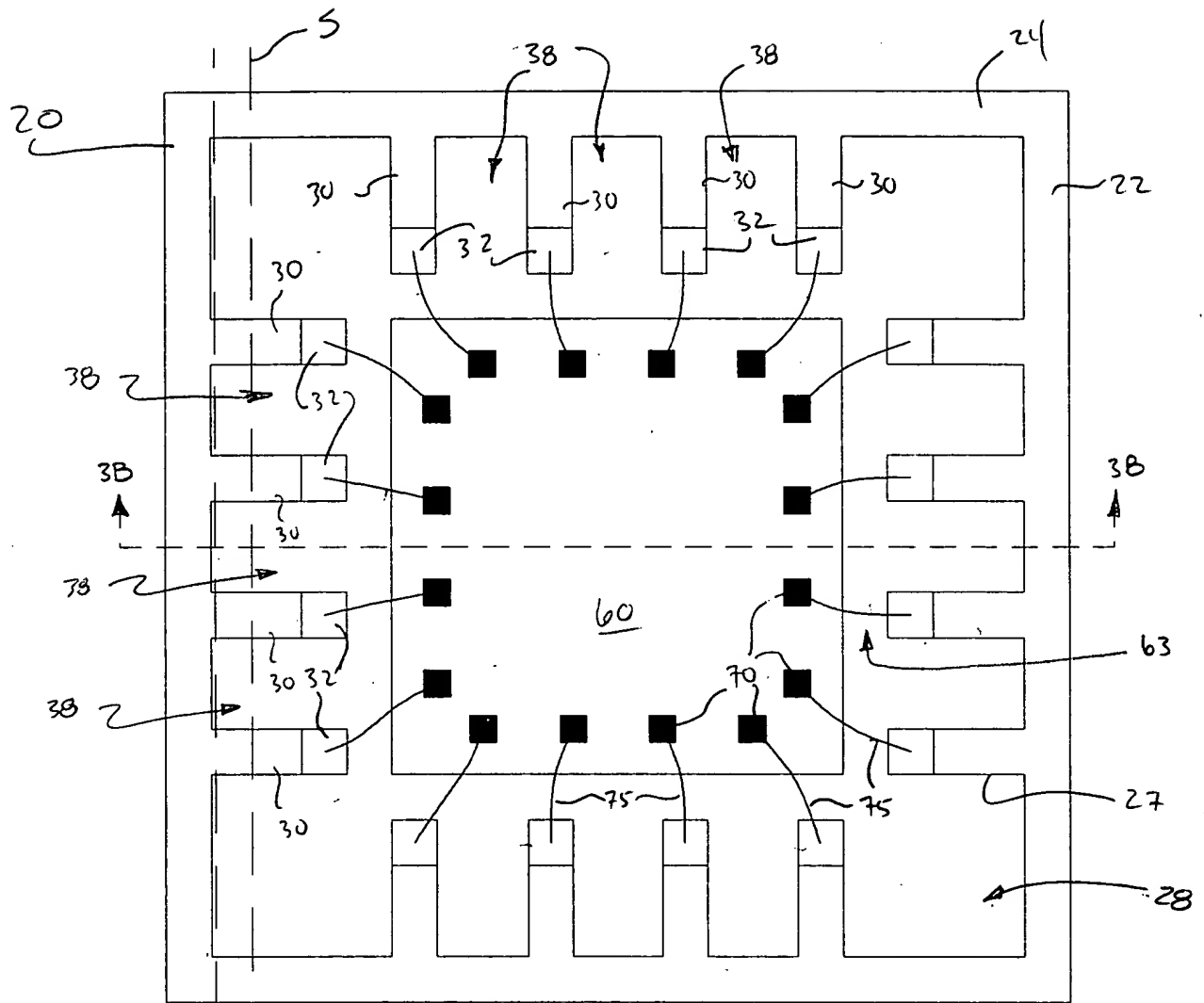


Fig. 3A

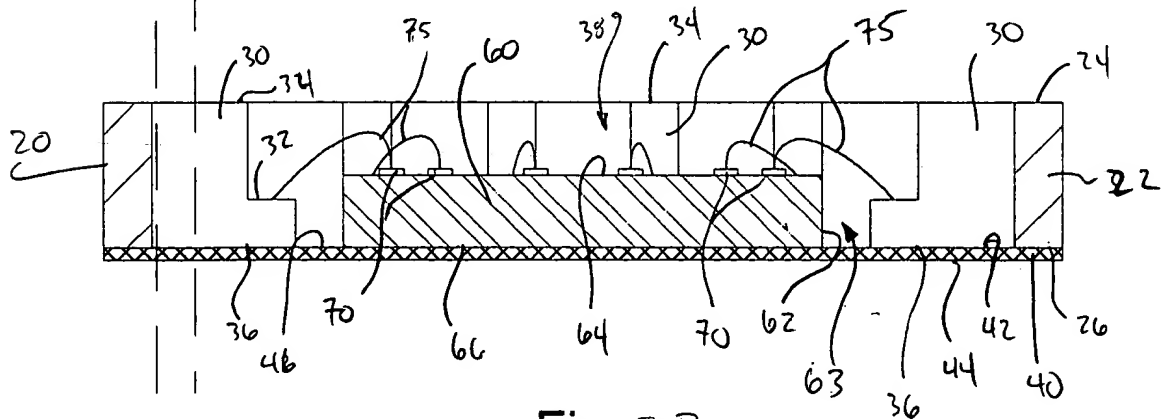
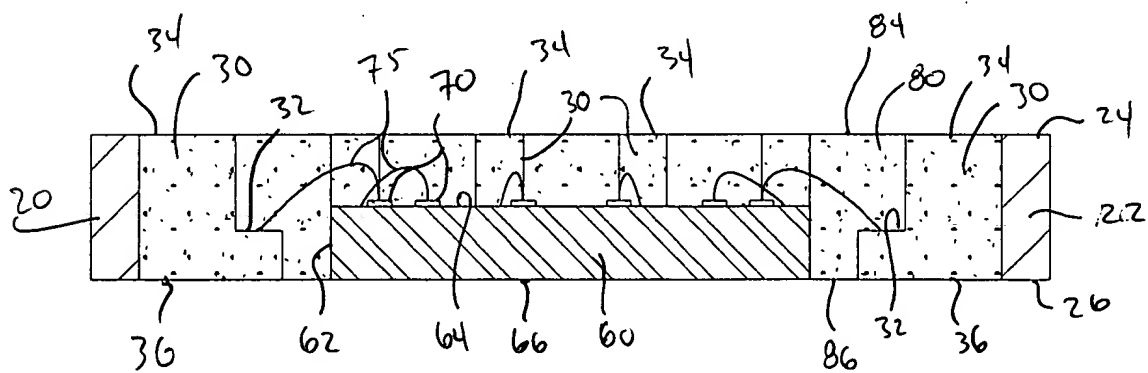
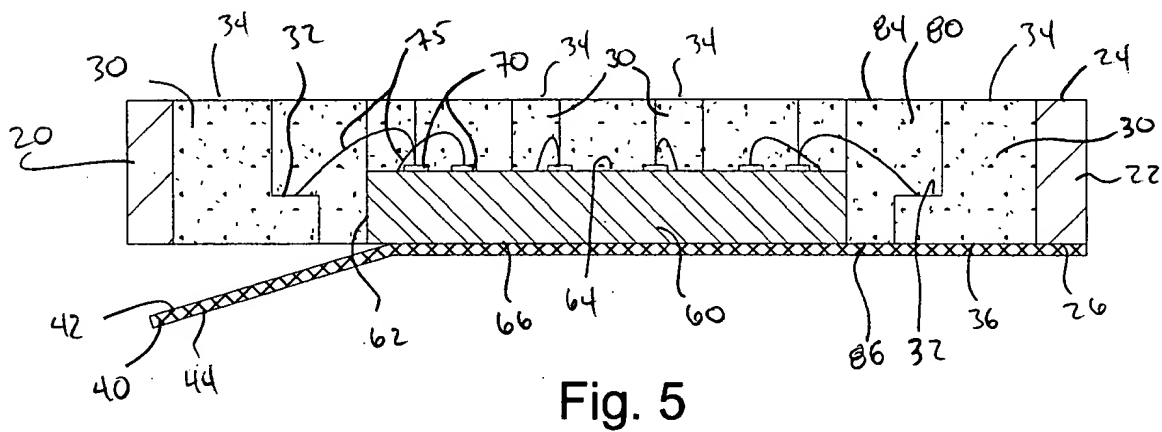
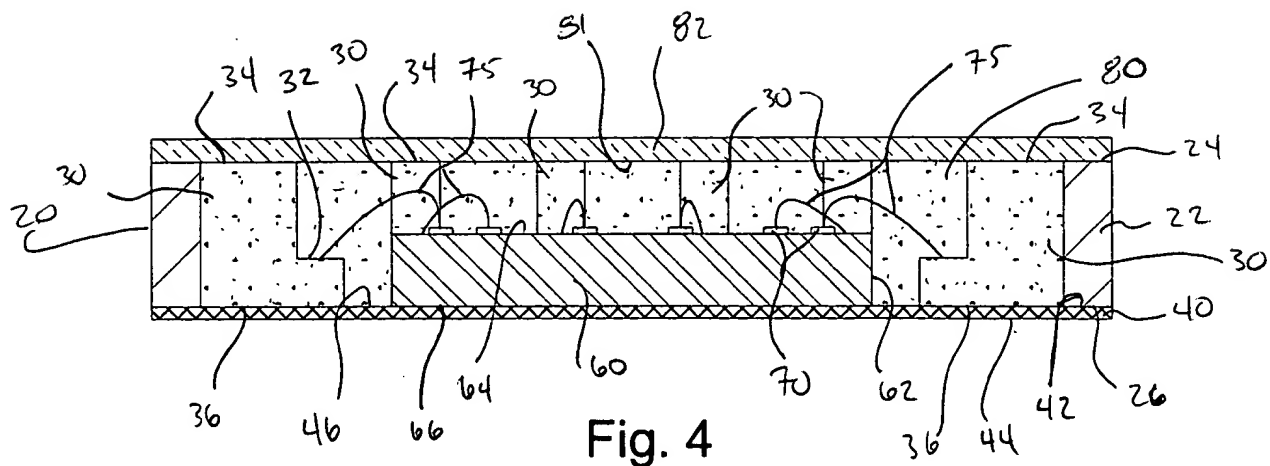


Fig. 3B



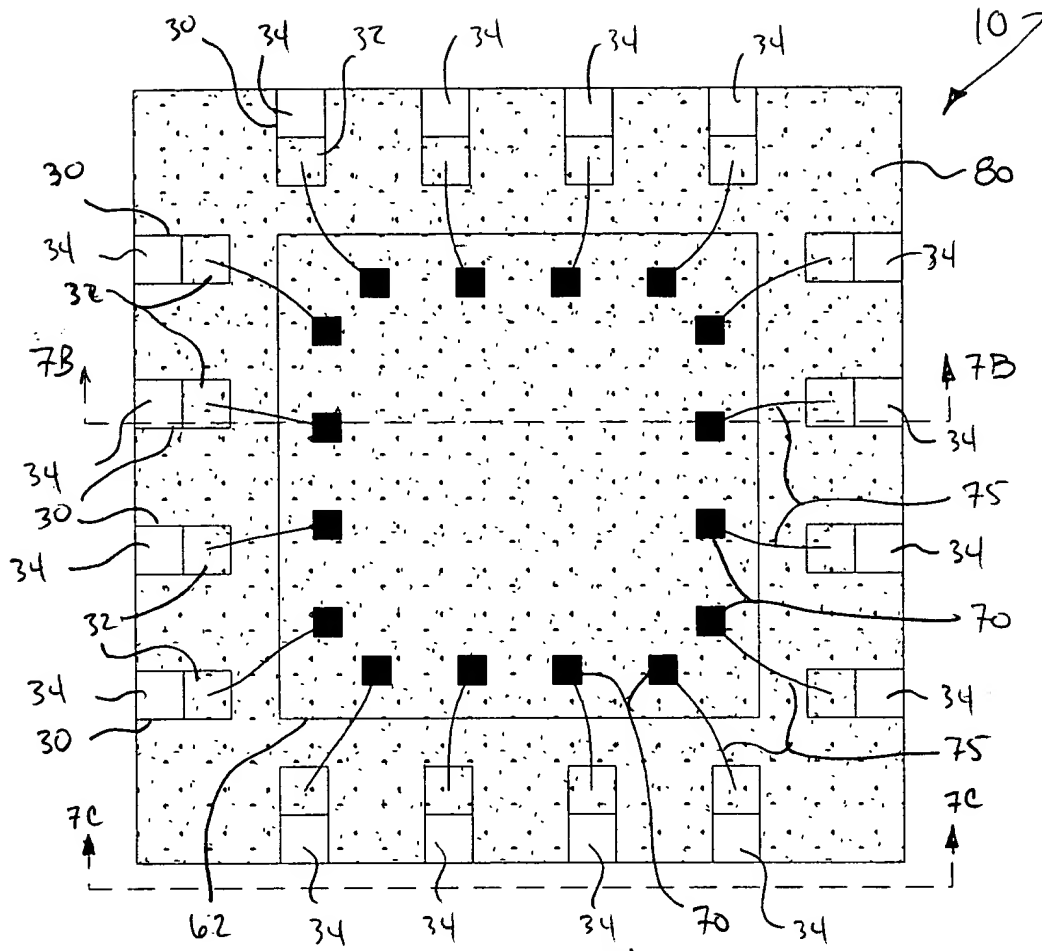


Fig. 7A

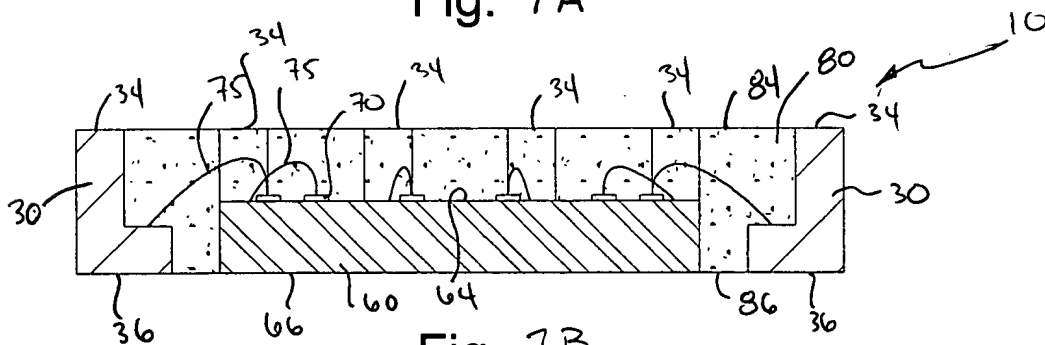


Fig. 7B

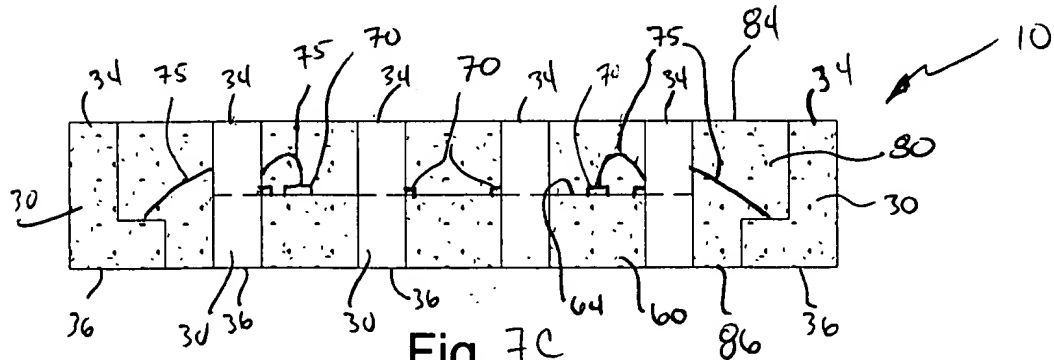


Fig. 7C

This diagram shows a cross-sectional view of a multi-layered electronic device assembly. The assembly consists of several layers and components:

- Top Layer (106):** A thin layer at the very top.
- Dielectric Layer (30b):** A layer below the top layer, containing several small, rounded features (34b).
- Conductive Layer (36b):** A layer below the dielectric layer, containing several small, rounded features (34b).
- Dielectric Layer (30a):** A layer below the conductive layer, containing several small, rounded features (34a).
- Conductive Layer (36a):** A layer below the dielectric layer, containing several small, rounded features (34a).
- Substrate (90):** A thick, hatched layer at the bottom.
- Interlayer Dielectric (92):** A thin layer between the conductive layers.
- Conductive Pads (91):** Small, rounded features on the conductive layers.
- Conductive Pads (93):** Small, rounded features on the substrate.
- Conductive Pads (94):** Small, rounded features on the dielectric layers.
- Conductive Pads (96):** Small, rounded features on the conductive layers.
- Conductive Pads (102):** Small, rounded features on the dielectric layers.

Fig. 8

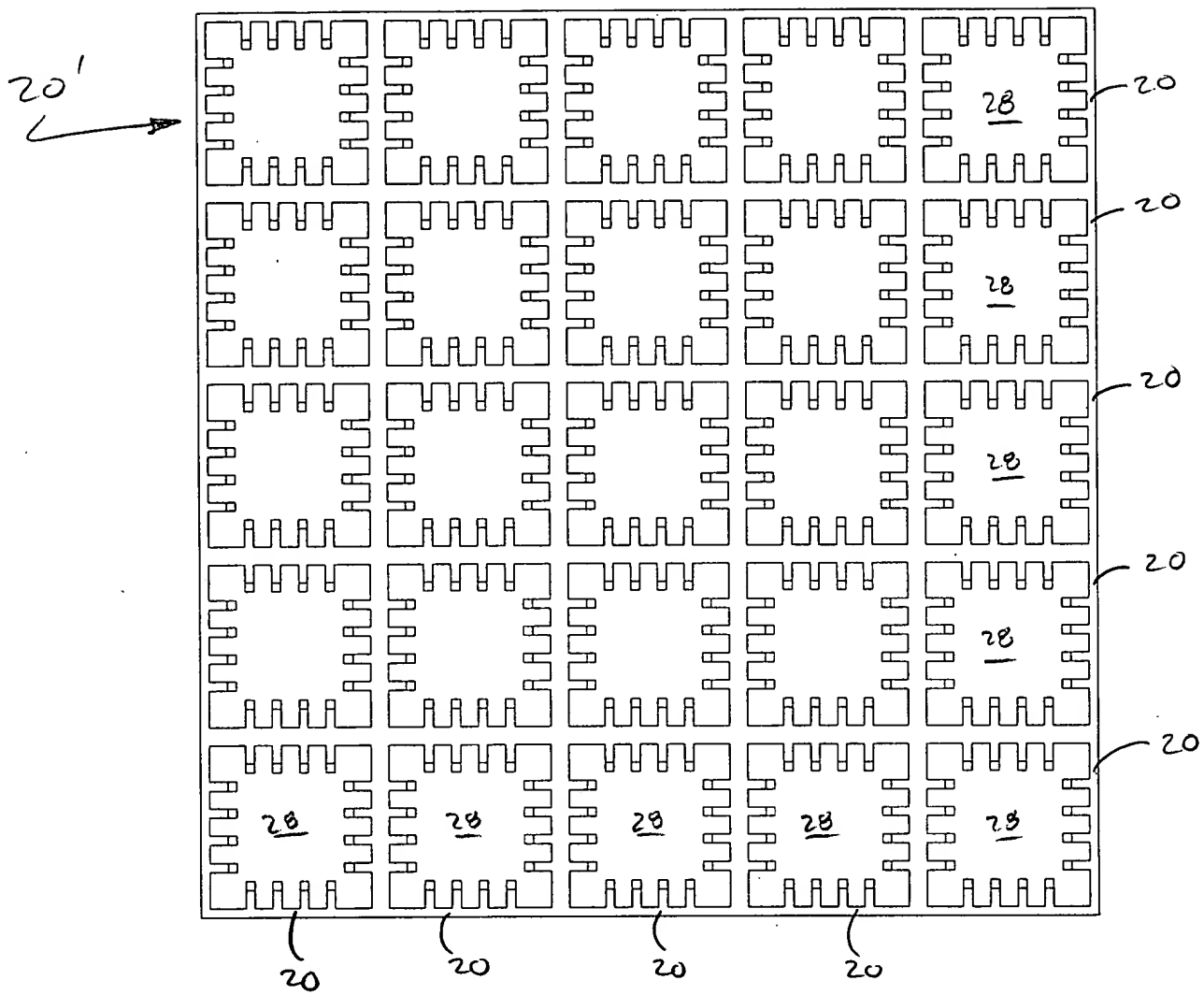


Fig. 9

FIG. 10A

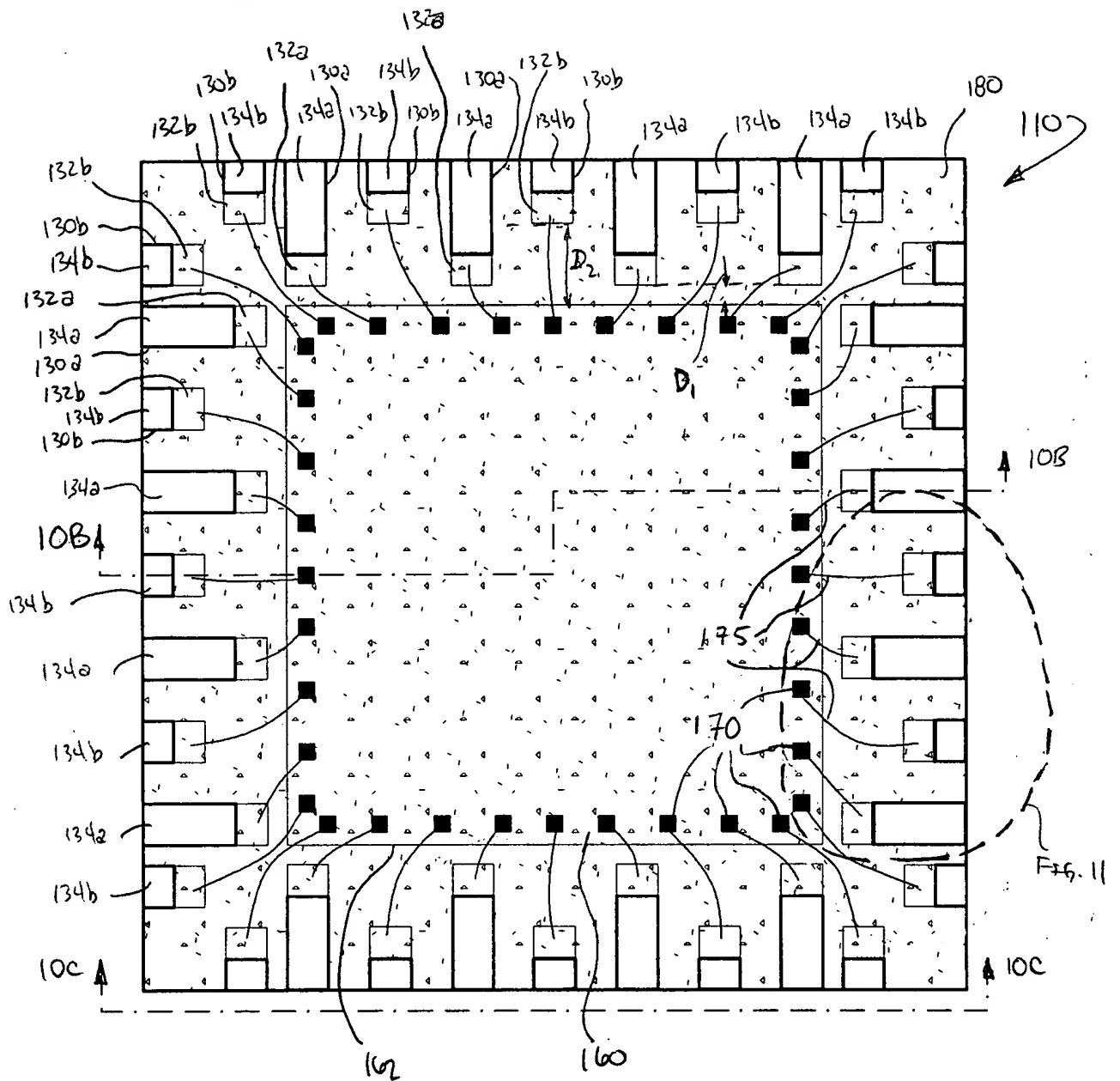


Fig. 10A

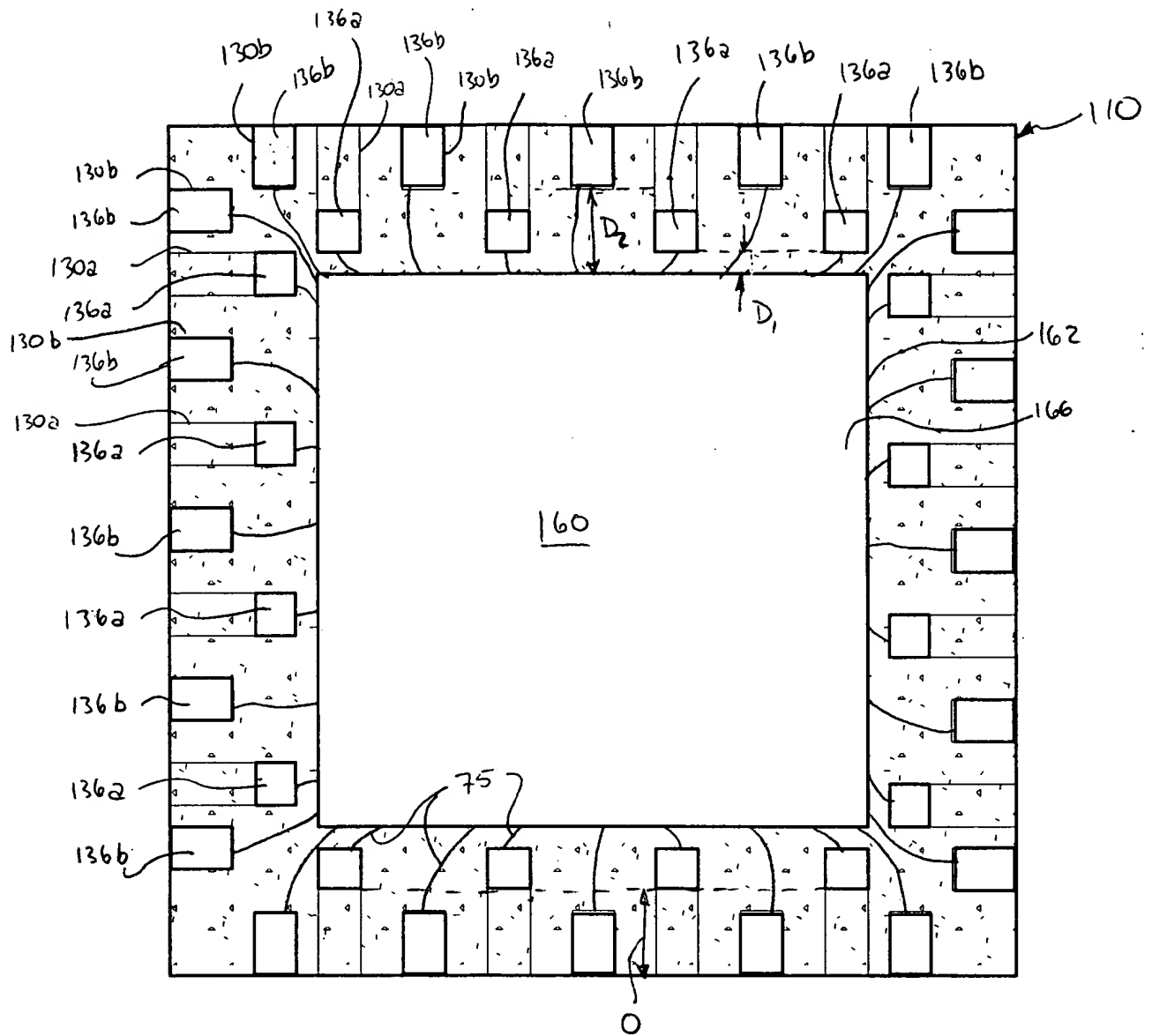


Fig. 10D

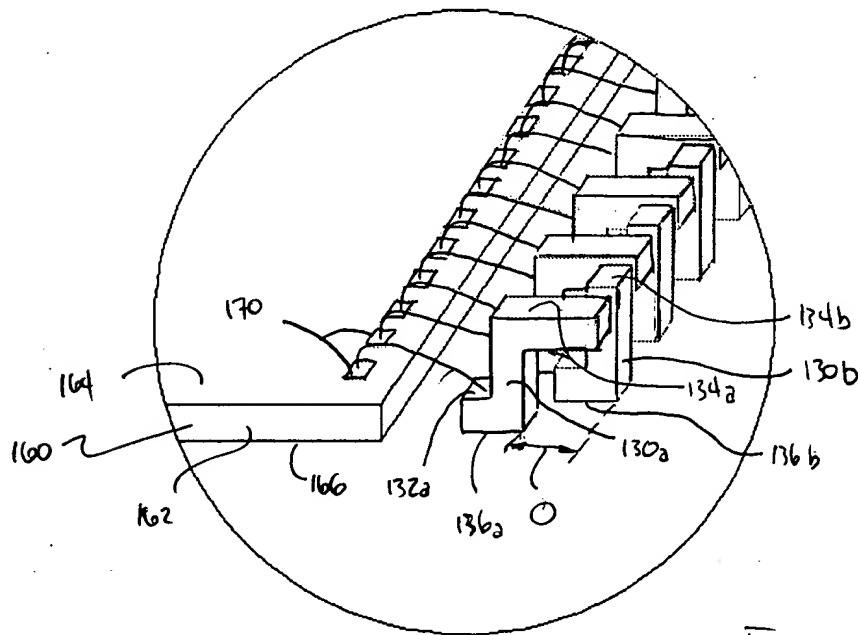
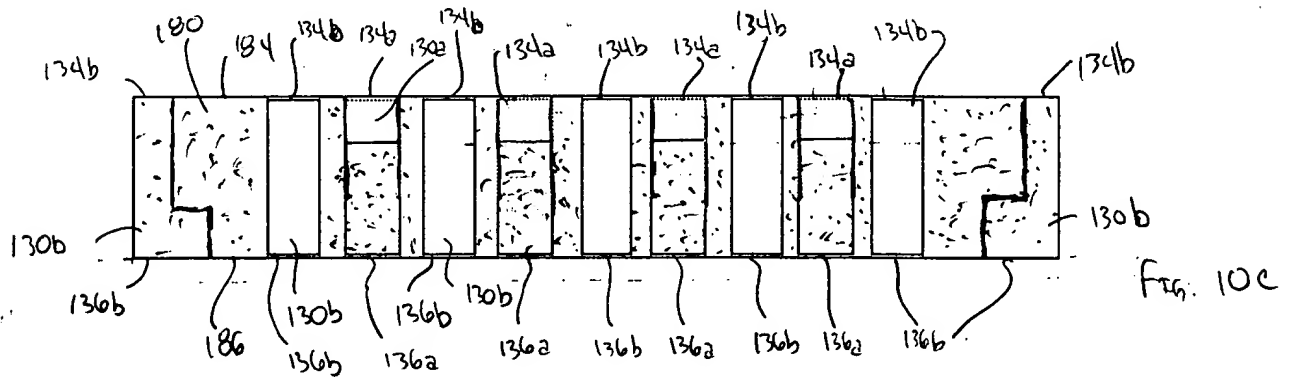
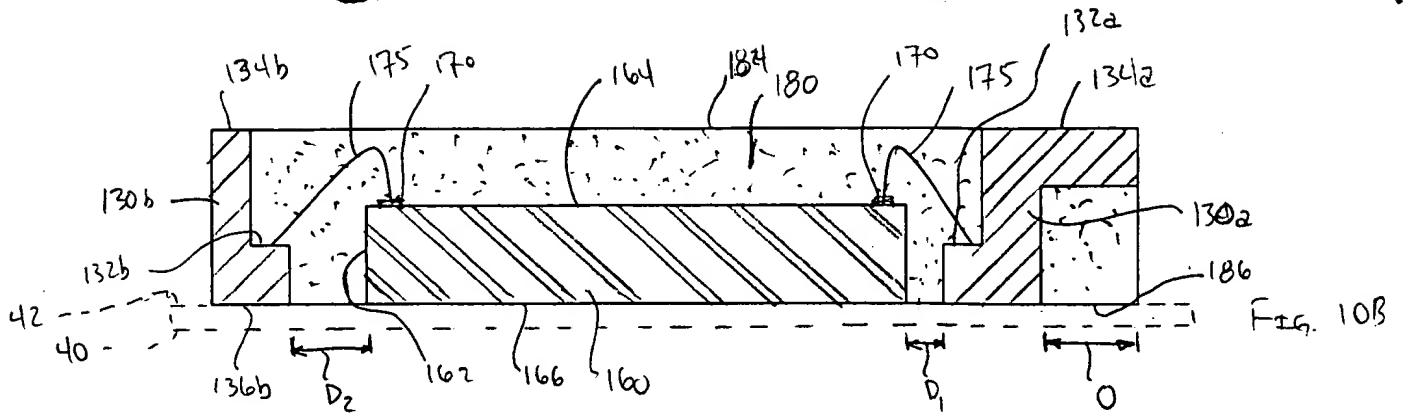
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FIG. 11